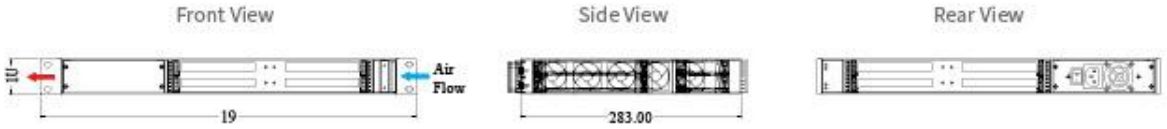
• 1U - Horizontal Configuration

Features

- EMC integrated system in 19" rack mount
- Aluminum enclosure
- Dimension: 1U (H) x 84T (W) x 283mm (D)
- 4 fans in a pluggable 1U fan unit
- 2-slot 6U CompactPCI backplane
- Front cage: 2-slot, 6U x 160mm
- Rear I/O: 2-slot, 6U x 80mm
- 250 W ATX power supply
- Customization is available

P/N: P-184283

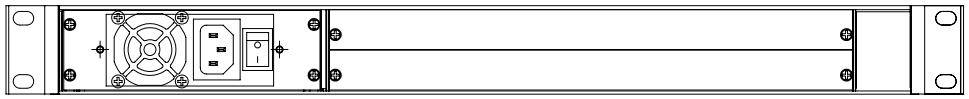
Mechanical Design

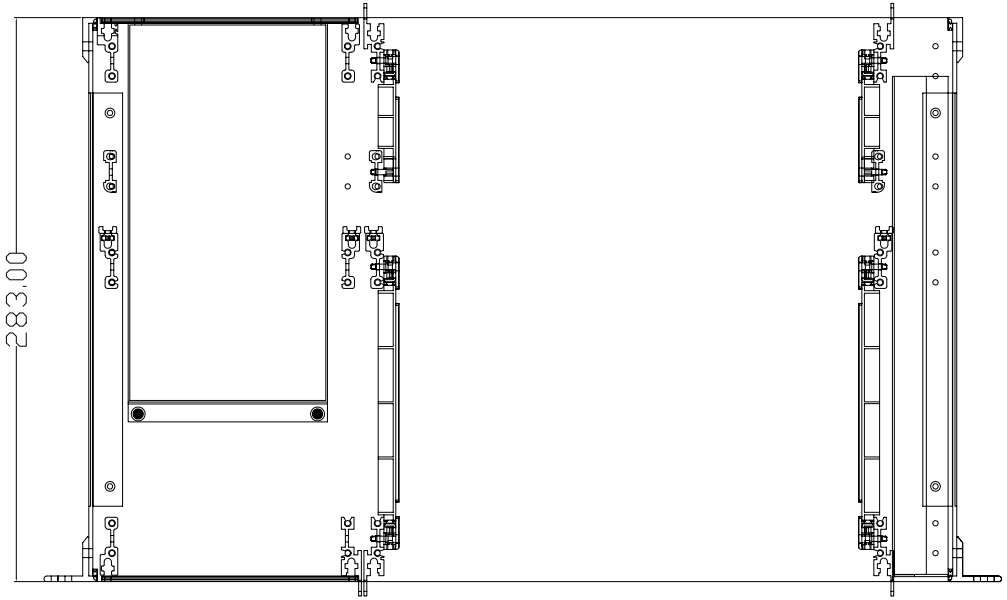


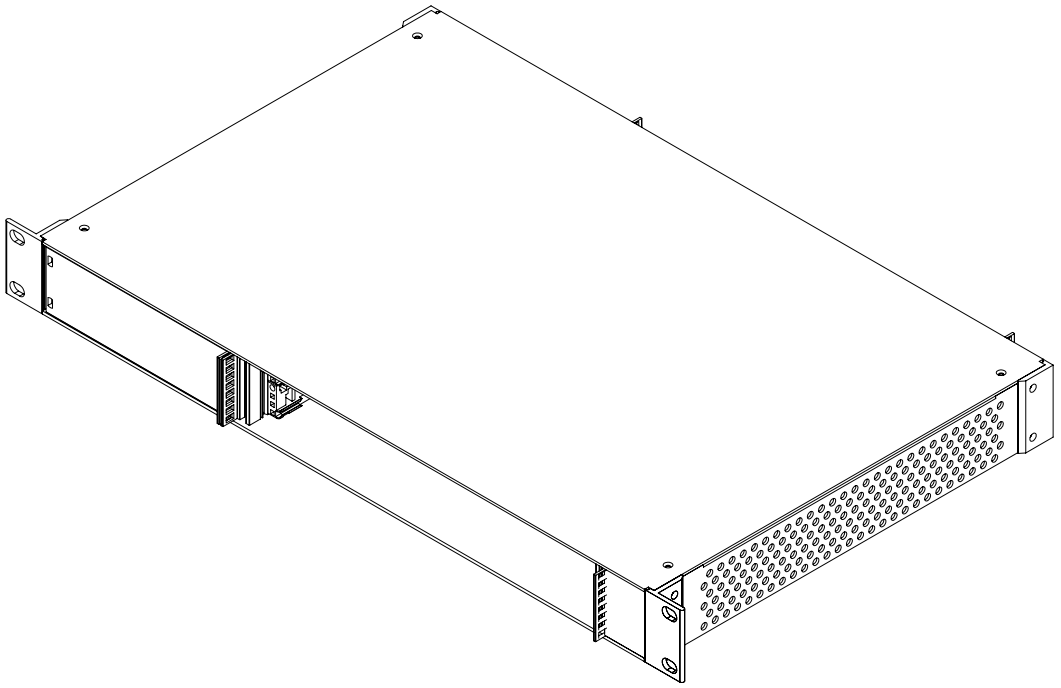
Specifications

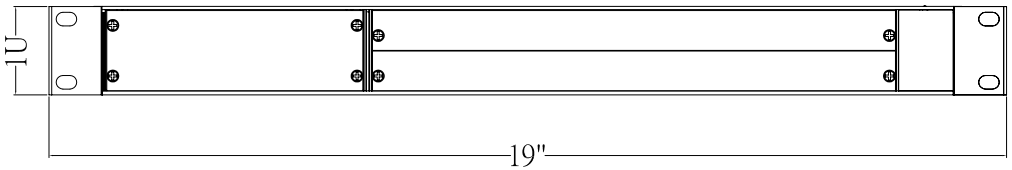
Fan Unit	Fan Mode	Bearing type	Nominal Voltage	DC 12 V
	Dimension	40 x 40 x 20 mm	Noise	30 dB
Backplane	2-slot 6U CompactPCI backplane(PICMG 2.16 or RICMG2.0 or 3.0 compliance)			
Power Supply ATX type	Output power	250 W		
	Output voltage	+5V/16A, +12V1/16A, +12V2/16A, -12V/0.8A, +3.3V/16.0A, +5vsb/2.5A Frequency 50/60HZ		
	Input voltage	100 - 240 VAC	Frequency	47 – 63 Hz

REVISIONS (變更記錄)				
版本	內　容	製圖	檢查	日期









公　差	原材料:	松驊精密工業有限公司 MAPSUKA INDUSTRIES CO., LTD.	品名: S184283	
標準(STD)...+/- 0.05	處理:			
半徑(RAD)...+/- 0.1	製圖者:	E-mail:mapsuka@mapsuka.com.tw	圖號:	版本: A
直徑(DIA)...+/- 0.1	確認者:	http://www.mapsuka.com.tw		
角度(ANG)...+/- 1°	日期:			
材料(MAT) 鈑金型+/- 0.2 鋁板 +/- 0.1	模號:	客戶	客戶圖號	視 圖 角 法 比例: 1:1
DIMS IN MM				

6U2S CompactPCI Backplane
User Manual

P/N: CPCI216R10U6S2-A1

1. Key Features :

- Conforms to PICMG 2.16 R1.0
- Supports Hot Swap feature of PICMG 2.1 R2.0
- CompactPCI Packet Switching Backplane (CompactPCI/PSB)
- Single Fabric PSB Topology
- Leverage IEEE 802.3-2000 1000BASE-T, providing physical and data link layers
- Physical interface at rates of 10, 100, or 1000 Mb/s on a slot-by-slot basis
- Support full-duplex bit rates of up to 2000 Mb/s per slot
- VI/O are user selectable to a +5V or +3.3V
- All signal lines characteristic impedance are set to 65Ω
- FR4 material PCB
- 2 m/m HM connector

2. Mechanical

The CompactPCI 32/64-Bit 2.16 Series backplanes are 10-layer PCBs which are 6U (262.05 mm) tall, 3.2 mm thick, 59.96 mm width. Two layers are dedicated ground layers. The backplanes are attached to the subrack using a series of screws along the top and bottom edges of the backplanes.

3. Backplane Pattern Connection Specification

Slot1 (S1) : System + Node
Slot2 (S2) :Peripheral + Fabric

3.1 CLK line

Slot No.	S1	S2
CLK No.	System	CLK0

3.2 GNT/REQ line

Slot No.	S1	S2
GNT/ REQ	System	GNT0/ REQ0

3.3 IDSEL line

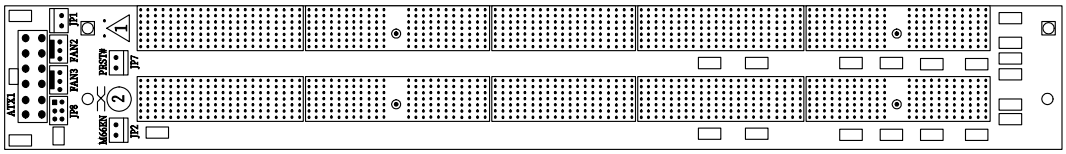
Slot No.	S1	S2
IDSEL	System	AD31

3.4 Interrupt line

Slot No.	S1	S2
Interrupt line	INTA#	INTD#
	INTB#	INTA#
	INTC#	INTB#
	INTD#	INTC#

4. Connectors and Jumpers

The relative position of connectors and jumpers on the backplane are shown as the following Figure.

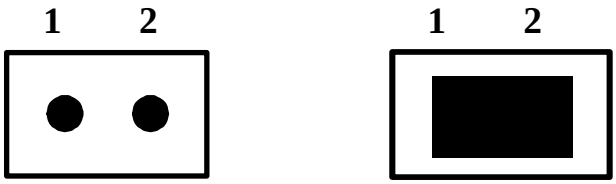


4.1 JP1 jumper

Power switch function.

4.2 JP2 jumper

M66EN, the 66MHz Enabling line, is defined as GND for 33 MHz backplane.



66 MHz **33 MHz**

4.3 JP7 jumper

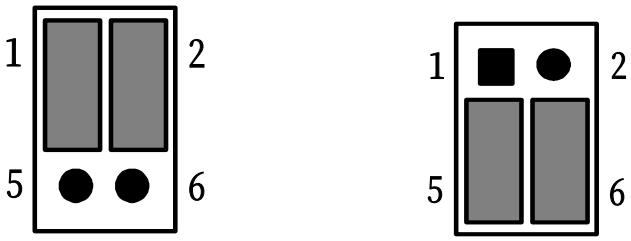
System reset function.

4.4 FAN2,FAN3 Connectors

Supply fans source (+12V)

4.5 JP8 Jumper

VI/O Selector



VI/O = 3.3V **VI/O = 5V**

4.6 ATX power connector

Pin	Power	Pin	Power
1	+3.3V	7	GND
2	+3.3V	8	+12V
3	GND	9	PSON#
4	+5V	10	-12V
5	GND	11	GND
6	PWOK	12	+5V

5. Backplane Pin Assignment Table

Table 5.1 CompactPCI System Slot P1 Connector Pin assignments

Pin	Z	A	B	C	D	E	F
25	GND	+5V	REQ64#(1)	ENUM#(2)	+3.3V	+5V	GND
24	GND	AD[1]	+5V	VI/O	AD[0]	ACK64#(1)	GND
23	GND	+3.3V	AD[4]	AD[3]	+5V	AD[2]	GND
22	GND	AD[7]	GND	+3.3V	AD[6]	AD[5]	GND
21	GND	+3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	VI/O	AD[11]	AD[10]	GND
19	GND	+3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	GND	SERR#	GND	+3.3V	PAR	C/BE[1]#	GND
17	GND	+3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND
16	GND	DEVSEL#	GND	VI/O	STOP#	LOCK#	GND
15	GND	+3.3V	FRAME#	IRDY#	GND	TRDY#	GND
J1-12~14 Keying Area							
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	GND	AD[21]	GND	+3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	GND	AD[23]	GND	AD[22]	GND
8	GND	AD[26]	GND	VI/O	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	GND	REQ0#	GND	+3.3V	CLK0	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	PCIRST#	GND	GNT0#	GND
4	GND	IPMB_PWR	HEALTHY#	VI/O	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	+5V	INTD#	GND

2	GND	TCK	+5V	TMS	TDO	TDI	GND
1	GND	+5V	-12V	TRST#	+12V	+5V	GND
Pin	Z	A	B	C	D	E	F

Table 5.2 CompactPCI System Slot P2 Connector Pin assignments

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	RSV	RSV	RSV	GND
20	GND	CLK5	GND	RSV	GND	RSV	GND
19	GND	GND	GND	RSV	RSV	RSV	GND
18	GND	BRSVP2A18	BRSVP2B18	BRSVP2C18	GND	BRSVP2E18	GND
17	GND	BRSVP2A17	GND	PRST#	REQ6#	GNT6#	GND
16	GND	BRSVP2A16	BRSVP2B16	DEG#	GND	BRSVP2E16	GND
15	GND	BRSVP2A15	GND	FAL#	REQ5#	GNT5#	GND
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	GND	AD[38]	GND	VI/O	AD[37]	AD[36]	GND
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	GND	AD[45]	GND	VI/O	AD[44]	AD[43]	GND
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	GND	AD[52]	GND	VI/O	AD[51]	AD[50]	GND
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	GND	AD[59]	GND	VI/O	AD[58]+	AD[57]	GND
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	GND	C/BE[5]#	GND	VI/O	C/BE[4]#	PAR64	GND
4	GND	VI/O	BRSVP2B4	C/BE[7]#	GND	C/BE[6]#	GND
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND
Pin	Z	A	B	C	D	E	F

Table 5.3 CompactPCI Peripheral Slot P1 Connector Pin assignments

Pin	Z	A	B	C	D	E	F
25	GND	+5V	REQ64#(1)	ENUM#(2)	+3.3V	+5V	GND
24	GND	AD[1]	+5V	VI/O	AD[0]	ACK64#(1)	GND
23	GND	+3.3V	AD[4]	AD[3]	+5V	AD[2]	GND

22	GND	AD[7]	GND	+3.3V	AD[6]	AD[5]	GND
21	GND	+3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	VI/O	AD[11]	AD[10]	GND
19	GND	+3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	GND	SERR#	GND	+3.3V	PAR	C/BE[1]#	GND
17	GND	+3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND
16	GND	DEVSEL#	GND	VI/O	STOP#	LOCK#	GND
15	GND	+3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
J1-12~14 Keying Area							
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	GND	AD[21]	GND	+3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	GND	AD[26]	GND	VI/O	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	GND	REQ#	GND	+3.3V	CLK	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	PCIRST#	GND	GNT#	GND
4	GND	IPMB_PWR	HEALTHY#	VI/O	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	+5V	INTD#	GND
2	GND	TCK	+5V	TMS	TDO	TDI	GND
1	GND	+5V	-12V	TRST#	+12V	+5V	GND
Pin	Z	A	B	C	D	E	F

Table 5.4 CompactPCI Peripheral Slot P2 Connector Pin assignments

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	RSV	RSV	RSV	RSV	RSV	GND
20	GND	RSV	RSV	RSV	GND	RSV	GND
19	GND	RSV	RSV	RSV	RSV	RSV	GND
18	GND	BRSVP2A18	BRSVP2B18	BRSVP2C18	GND	BRSVP2E18	GND
17	GND	BRSVP2A17	GND	RSV	RSV	RSV	GND
16	GND	BRSVP2A16	BRSVP2B16	RSV	GND	BRSVP2E16	GND
15	GND	BRSVP2A15	GND	RSV	RSV	RSV	GND
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	GND	AD[38]	GND	VI/O	AD[37]	AD[36]	GND
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	GND	AD[45]	GND	VI/O	AD[44]	AD[43]	GND

10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	GND	AD[52]	GND	VI/O	AD[51]	AD[50]	GND
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	GND	AD[59]	GND	VI/O	AD[58]+	AD[57]	GND
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	GND	C/BE[5]#	GND	VI/O	C/BE[4]#	PAR64	GND
4	GND	VI/O	BRSVP2B4	C/BE[7]#	GND	C/BE[6]#	GND
3	GND	RSV	GND	RSV	RSV	RSV	GND
2	GND	RSV	RSV	UNC	RSV	RSV	GND
1	GND	RSV	GND	RSV	RSV	RSV	GND
Pin	Z	A	B	C	D	E	F

Table 5.5 Fabric Slot P3 Connector Pin assignments

Pin	Z	A	B	C	D	E	F
19	GND	SGA4	SGA3	SGA2	SGA1	SGA0	GND
18	GND	LPf_DA+	LPf_DA-	GND	LPf_DC+	LPf_DC-	GND
17	GND	LPf_DB+	LPf_DB-	GND	LPf_DD+	LPf_DD-	GND
16	GND	LP8_DA+	LP8_DA-	GND	LP8_DC+	LP8_DC-	GND
15	GND	LP8_DB+	LP8_DB-	GND	LP8_DD+	LP8_DD-	GND
14	GND	LP7_DA+	LP7_DA-	GND	LP7_DC+	LP7_DC-	GND
13	GND	LP7_DB+	LP7_DB-	GND	LP7_DD+	LP7_DD-	GND
12	GND	LP6_DA+	LP6_DA-	GND	LP6_DC+	LP6_DC-	GND
11		LP6_DB+	LP6_DB-	GND	LP6_DD+	LP6_DD-	
10		LP5_DA+	LP5_DA-	GND	LP5_DC+	LP5_DC-	
9		LP5_DB+	LP5_DB-	GND	LP5_DD+	LP5_DD-	
8	GND	LP4_DA+	LP4_DA-	GND	LP4_DC+	LP4_DC-	GND
7	GND	LP4_DB+	LP4_DB-	GND	LP4_DD+	LP4_DD-	GND
6	GND	LP3_DA+	LP3_DA-	GND	LP3_DC+	LP3_DC-	GND
5	GND	LP3_DB+	LP3_DB-	GND	LP3_DD+	LP3_DD-	GND
4	GND	LP2_DA+	LP2_DA-	GND	LP2_DC+	LP2_DC-	GND
3	GND	LP2_DB+	LP2_DB-	GND	LP2_DD+	LP2_DD-	GND
2	GND	LP1_DA+	LP1_DA-	GND	LP1_DC+	LP1_DC-	GND
1	GND	LP1_DB+	LP1_DB-	GND	LP1_DD+	LP1_DD-	GND
Pin	Z	A	B	C	D	E	F

Table 5.6 Node Slot P3 Connector Pin assignments

Pin	Z	A	B	C	D	E	F
19	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
18	GND	LPa_DA+	LPa_DA-	GND	LPa_DC+	LPa_DC-	GND
17	GND	LPa_DB+	LPa_DB-	GND	LPa_DD+	LPa_DD-	GND
16	GND	LPb_DA+	LPb_DA-	GND	LPb_DC+	LPb_DC-	GND
15	GND	LPb_DB+	LPb_DB-	GND	LPb_DD+	LPb_DD-	GND
14	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
13	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
12	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
11		BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	
10		BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	
9		BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	
8	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
7	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
6	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
5	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
4	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
3	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
2	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
1	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
Pin	Z	A	B	C	D	E	F